REMARKS

Applicant's invention is directed to a semiconductor device in which a layer of silicon oxide has been doped with hydrogen ions deposited by a plasma source ion implantation process such that a subsequent layer of polycrystalline silicon formed on the layer of silicon dioxide has a smooth morphology and is free of sputtered metal contaminants. Claims 9-12 and 14 are presently pending in this application.

In the most recent Office Action, the Examiner rejected claims 9-12 and 14 under 35 USC §112, ¶2, as being indefinite. Specifically, the Examiner opined that the phrase "free of sputtered metal contaminants" was unclear "because one cannot ascertain the meets [sic, metes] and bounds of the limitation." The Examiner posited several possible alternative meanings for the phrase and also asserted that the specification did not objectively define what level of contaminants would be considered to be "free of sputtered metal contaminants."

As the Examiner must be aware, terms in a claim are to be read in light of the specification, the prior art, and how one skilled in the particular art would understand such terminology. MPEP §2173.02. Absolute precision and clarity are not required. Nor is there a requirement that numerical or percentage limitations be placed on claim terms. See, e.g., *In re Marosi*, 218 USPQ 289 (Fed. Cir. 1983) (phrase "essentially free of alkali metal" held definite where specification provided general guidance; applicant not required to put a numerical value on the limitation). Applying those basic principles to the present application and claims, the specification defines the problem of metal contamination on page 1. More specifically, it is explained that a Kaufman ion source sputters metal from a grid and the metal becomes implanted in the target (e.g., a layer of silicon dioxide) causing the target to become contaminated from the sputtered metal. See page 1, lines 17-23.

In addition, the specification explains that using PSII reduces metal contamination on a target substrate because it does not use a metal grid. See page 10, lines 9-13. Thus, in light of the specification, it is evident to one of ordinary skill in the art that the phrase "free of sputtered metal contaminants" means that the layer of silicon dioxide (or

semiconductor substrate in the case of claim 14) has no sputtered metal atoms present. Neither the specification nor the claims recite that the layer is free from all metal contaminants ("free from sputtered metal contaminants"). However, the specification is clear that use of PSII to implant hydrogen ions reduces metal contamination because it eliminates the metal grid that was present in prior art Kaufman ion implanting processes, thus eliminating *sputtered* metal contaminants from the surface of the layer. Applicant submits that the claims are definite and in compliance with §112.

Also, claim 14 was rejected as indefinite, with the Examiner questioning the proper position of the gate oxide in the claimed structure. Claim 14 has been amended to clarify that the gate oxide is formed in the semiconductor substrate. Basis for this claim limitation may be found in the specification at page 10, lines 25-26. The claim language has also been clarified to recite that the source and drain regions are also formed in the semiconductor substrate. Finally, applicant has deleted the offending phrase "having hydrogen ions implanted therein ...". Applicant submits that claim 14 as amended is definite and is in compliance with §112.

Also in the Office Action, the Examiner rejected claims 9-12 and 14 under 35 USC §112, ¶1, as not being enabled. Again, the Examiner questioned the phrase "free of sputtered metal contaminants," and concluded that one skilled in this art would not be able to form the claimed structure. Applicant strongly disagrees.

Initially, applicant has discussed in the specification the prior art process of ion implantation that uses a Kaufman ion source. Such a source employs a metal grid and thus results in metal contaminants being sputtered from the grid onto the semiconductor substrate. See, page 1, lines 17-23. The specification also explains a process using PSII that does not employ a metal grid and thus does not result in any metal be sputtered onto the semiconductor substrate during ion implantation. See, page 10, lines 6-13. The claims do not recite a structure in which the silicon dioxide (semiconductor in claim 14) layer is free from all metal contaminants, only that it is "free from sputtered metal contaminants."

The Examiner may be correct that there are a number of possible sources for metal contaminants in a semiconductor fabrication process. However, none of these

speculative sources represent sources of *sputtered* metals and none would be "sputtered" onto the layer during the PSII process. The Examiner states that "[t]he specification has not enabled a process in which no metal atoms will be present in the ion source apparatus and thus it would be expected that there would be some level of metal sputtered into the target." The Examiner misapprehends the meaning of "sputtered" as one skilled in this art would understand that term. Sputtering involves the deposition of material by bombarding a metal target with energized ions that "knock" atoms off the target and onto a substrate. The art-recognized technique of plasma source ion implantation does not involve sputtering of metal atoms from a target onto a substrate. Contrary to the Examiner's assertions, plasma source ion implantation does not involve sputtering as that term is understood in this art. There is no solid metal target used in the process. Hydrogen gas is ionized and forms a plasma. Application of an electrical bias causes the ionized plasma to be accelerated into the surface of the substrate.

Thus, applicant is not claiming a layer that is free from all metal contaminants, only free of *sputtered* metal contaminants. Applicant is not obligated to enable the former because that is not claimed; the latter is enabled by the specification as filed. Applicant submits that the rejection is not well taken and should be withdrawn.

Also in the Office Action, the Examiner rejected claim 9 under 35 USC §102 as anticipated by "Applicant's admitted prior art." The crux of this rejection appears to reside in the Examiner's assertion that while the "admitted prior art" does not explicitly state the layer of silicon dioxide is "free of sputtered metal contaminants," the limitation "is considered implicitly understood." The Examiner further asserts that, "It is implicitly understood that there are no uranium metal atoms sputtered into the oxide layer and thus it is free of sputtered metal contaminants."

Applicant does not understand the Examiner's reference to uranium, unless it is in conjunction with the Examiner's asserted (and incorrect) construction of the phrase "free of sputtered metal contaminants" as meaning "free of sputtered metal contaminants of a certain species." Initially, the Examiner cannot arbitrarily construe claim terminology in a manner clearly not intended and then use that incorrect construction as basis for a rejection. The prior art structure that is discussed at page 1 of the specification very

clearly is stated to contain sputtered metal contaminants. The Examiner's assertions to the contrary are directly at odds with the evidence of record. As discussed above, the phrase "free of sputtered metal contaminants" is properly construed to mean that the layer of silicon dioxide (or semiconductor substrate in the case of claim 14) has no sputtered metal atoms present. The prior art discussed at page 1 of the specification clearly does, and thus cannot anticipate claim 9.

Also in the Office Action, the Examiner rejected claims 10-12 under 35 USC §103 as unpatentable over Burns et al in view of "admitted prior art." Again, the crux of this rejection is the Examiner's incorrect construction of the phrase "free of sputtered metal contaminants." As discussed above, the prior art that is discussed on page 1 of the specification very clearly states that metal is sputtered from a grid and becomes implanted in the target object, thereby contaminating it. Thus, using a Kaufman ion source to implant ions into the FET of Burns et al would not result in the claimed invention. The rejection is not well taken and should be withdrawn.

Also in the Office Action, the Examiner rejected claim 14 under 35 USC §103 as unpatentable over Murata in view of admitted prior art. Again, as before, the crux of the rejection is the Examiner's incorrect construction of the phrase "free of sputtered metal contaminants." As discussed above, the prior art that is discussed on page 1 of the specification very clearly states that metal is sputtered from a grid and becomes implanted in the target object, thereby contaminating it. Thus, using a Kaufman ion source to implant ions into the TFT of Murata would not result in the claimed invention. The rejection is not well taken and should be withdrawn.

For all of the reasons stated above, applicant submits that claims 9-12 and 14 as amended are in compliance with §112 of the statute and are patentable over the prior art of record. Early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,

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